OIPE IAP68
DEC 19 2007
PATENT & TRADEMARK OFFICE

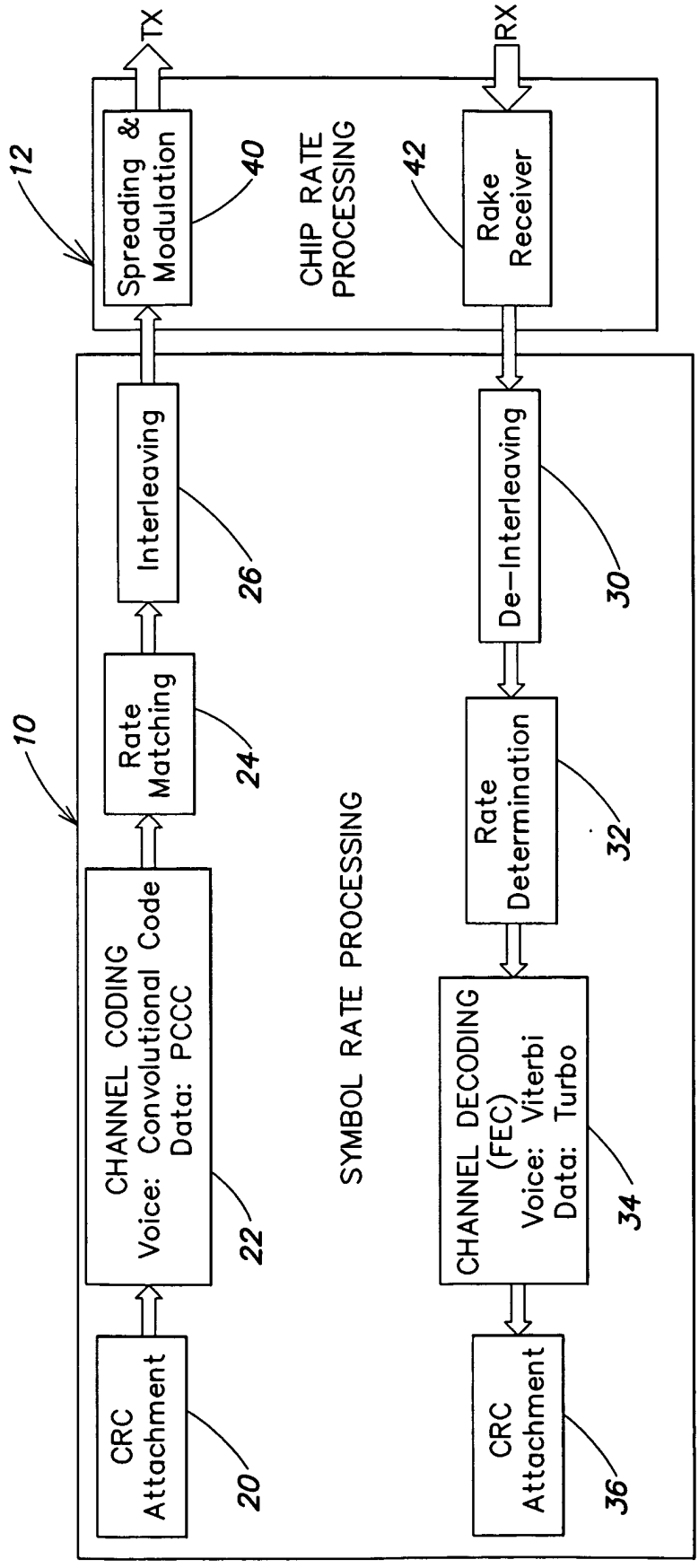

FIG. 1

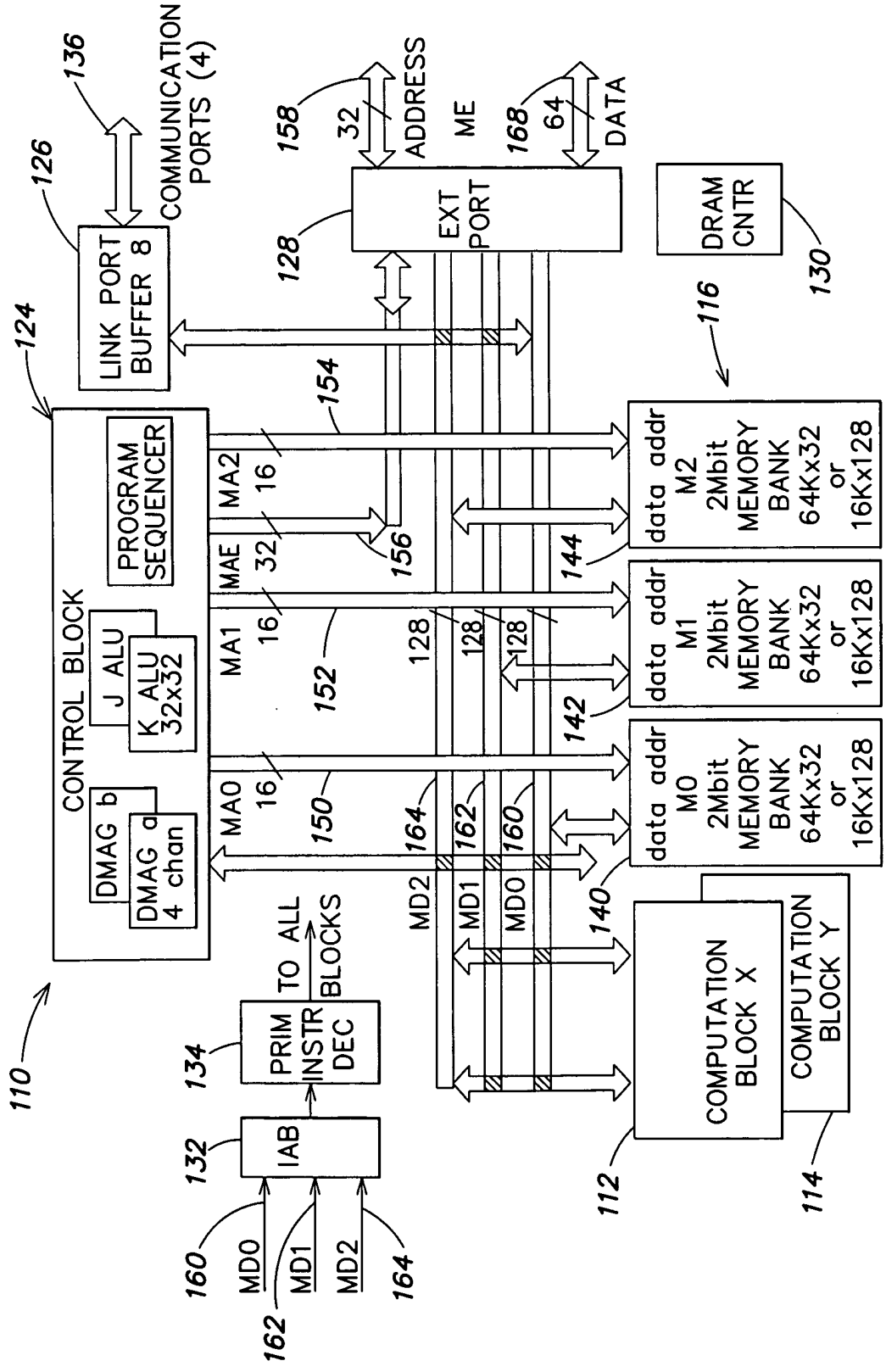
110
CONTROL BLOCK
PROGRAM SEQUENCER
J ALU
K ALU 32x32
DMAG b
DMAG a 4 chan
124
126
LINK PORT BUFFER 8
136
COMMUNICATION PORTS (4)
128
EXT PORT
158
32
ADDRESS
168
64
DATA
ME
130
DRAM CNTR
116
MA2
MAE
MA1
MA0
16
32
154
156
152
150
144
142
140
128
164
162
160
MD2
MD1
MD0
data addr M2 2Mbit MEMORY BANK 64Kx32 or 16Kx128
data addr M1 2Mbit MEMORY BANK 64Kx32 or 16Kx128
data addr M0 2Mbit MEMORY BANK 64Kx32 or 16Kx128
TO ALL BLOCKS
PRIM INSTR DEC
134
IAB
132
160
MD0
162
MD1
MD2
164
COMPUTATION BLOCK X
112
COMPUTATION BLOCK Y
114

FIG. 2

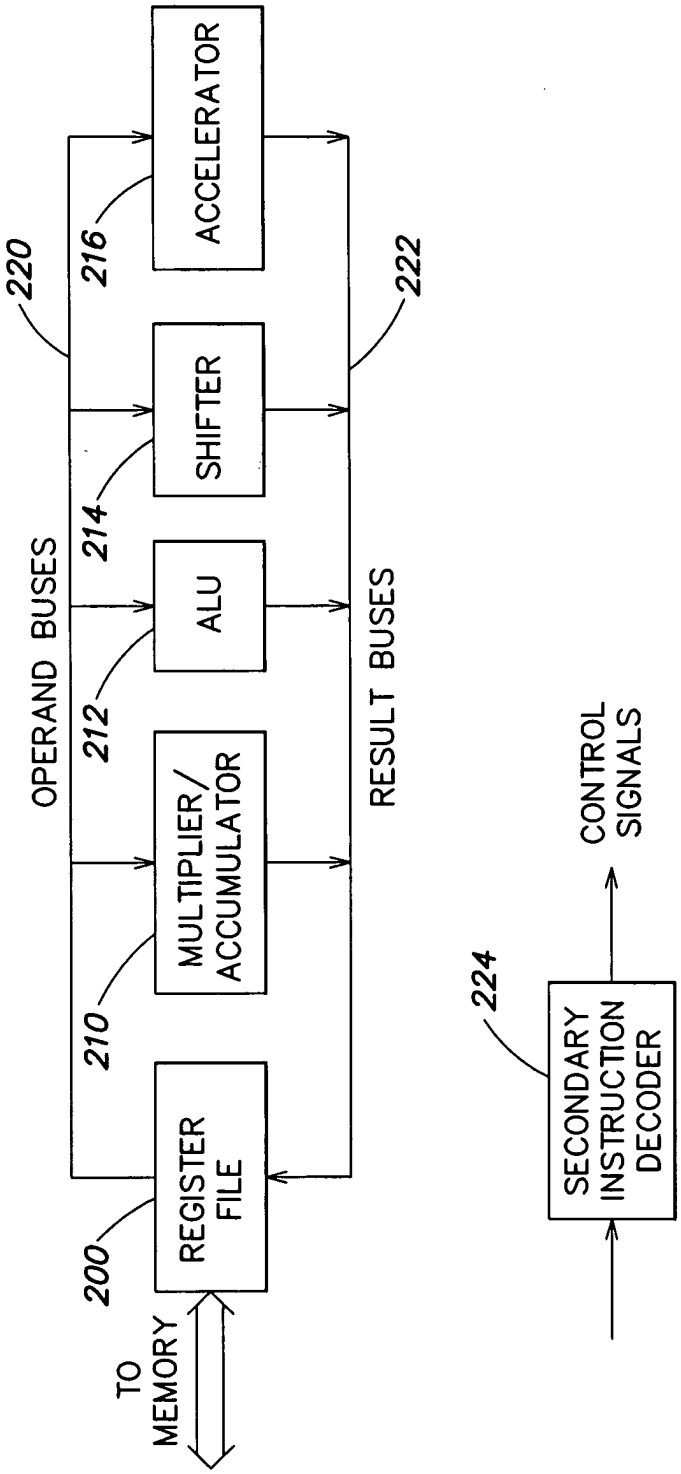
ACCELERATOR
SHIFTER
ALU
MULTIPLIER/
ACCUMULATOR
REGISTER
FILE
TO
MEMORY
OPERAND BUSES
RESULT BUSES
220
222
216
214
212
210
200
224
SECONDARY
INSTRUCTION
DECODER
CONTROL
SIGNALS

FIG. 3

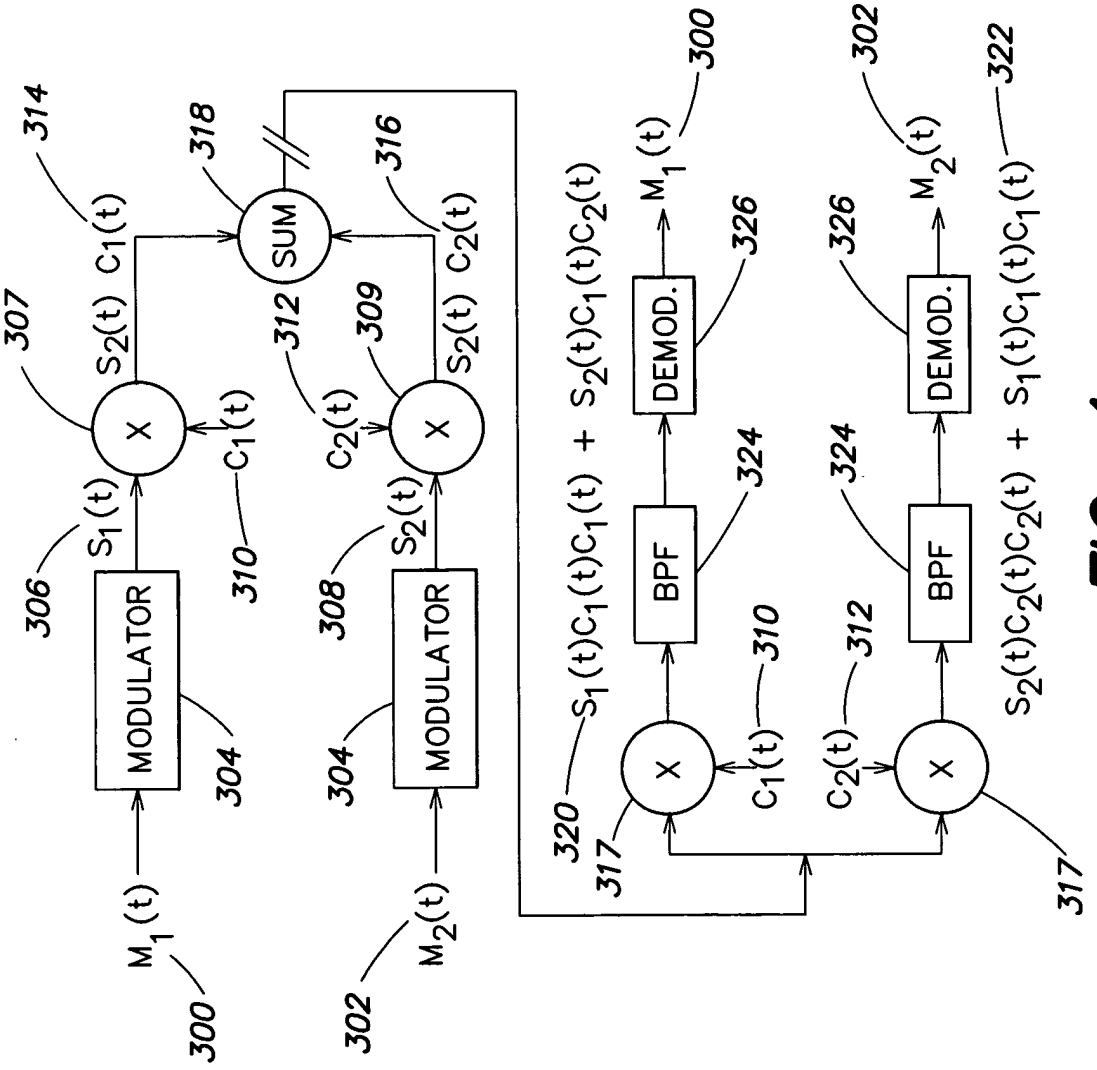
300
$M_1(t)$
MODULATOR
304
306
$S_1(t)$
307
X
$S_2(t)$ $C_1(t)$
314
310
$C_1(t)$
302
$M_2(t)$
MODULATOR
304
308
$S_2(t)$
312
$C_2(t)$
309
X
$S_2(t)$ $C_2(t)$
316
318
SUM
320
$S_1(t)C_1(t)C_1(t) + S_2(t)C_1(t)C_2(t)$
317
X
$C_1(t)$
310
BPF
324
DEMOD.
326
$M_1(t)$
300
$C_2(t)$
312
X
$S_2(t)C_2(t)C_2(t) + S_1(t)C_1(t)C_1(t)$
317
322
BPF
324
DEMOD.
326
$M_2(t)$
302

FIG. 4

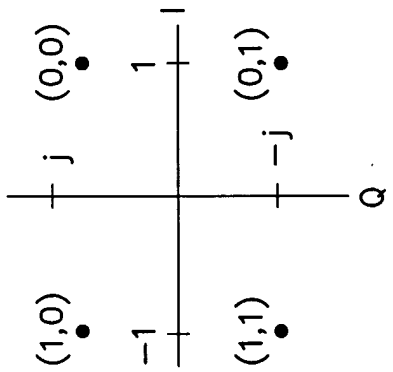

FIG. 6

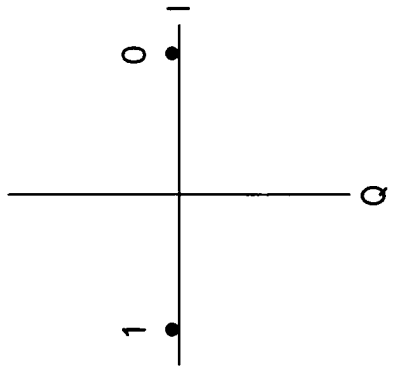

FIG. 5

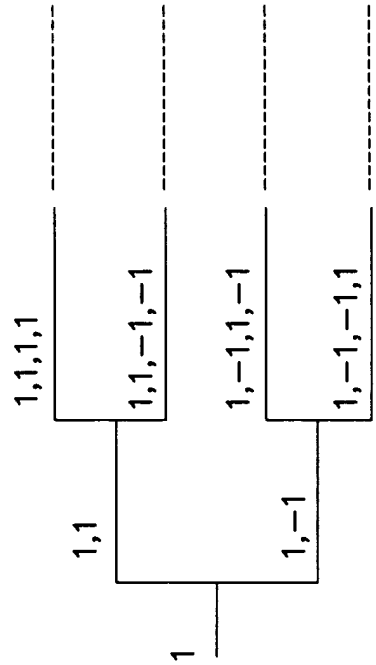

FIG. 7

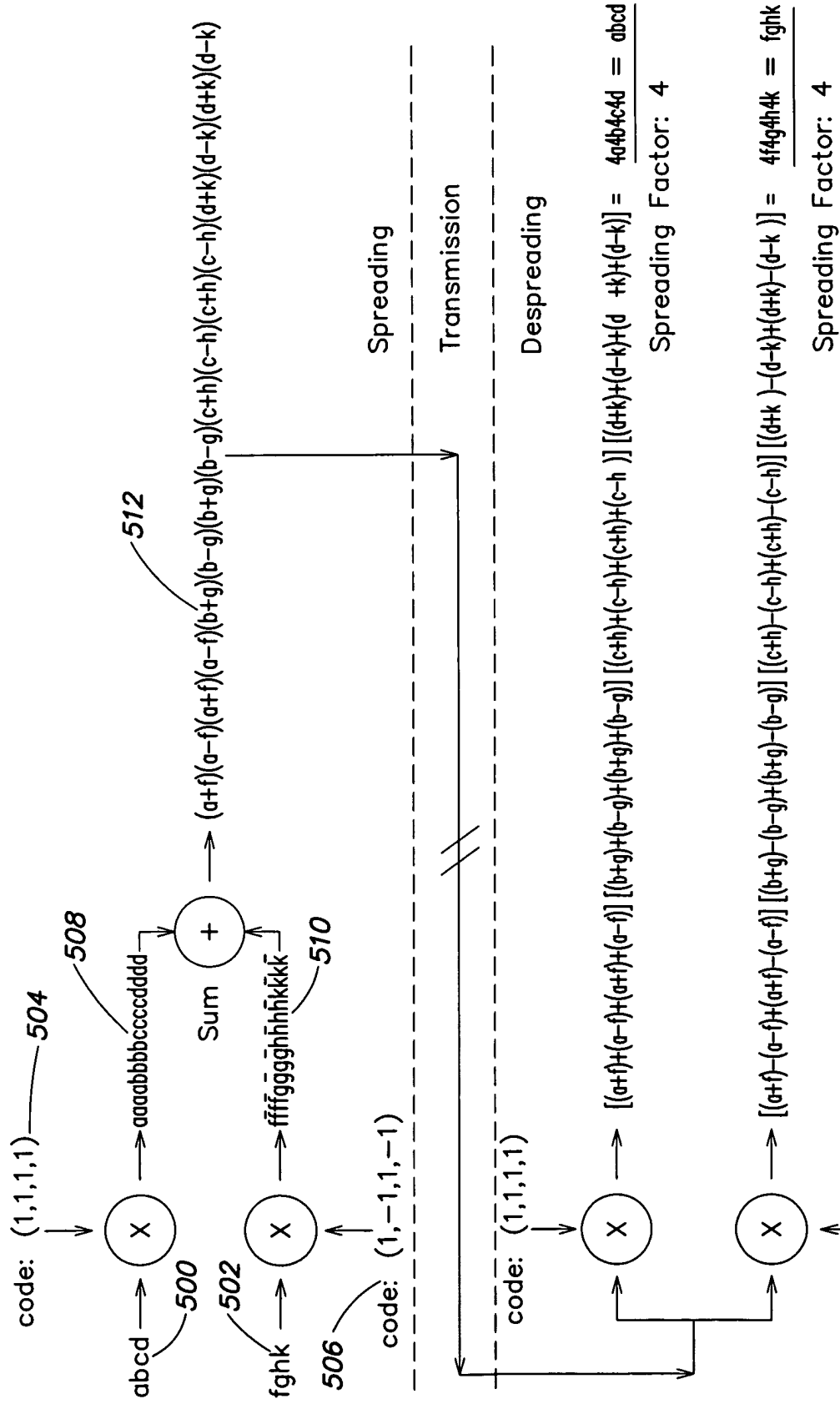
code: (1,1,1,1)
504
abcd
500
aaaabbbbccccdddd
508
fghk
502
ffffgggghhhhkkkk
510
code: (1,−1,1,−1)
506
Sum
+
(a+f)(a−f)(a+f)(a−f)(b+g)(b−g)(b+g)(b−g)(c+h)(c−h)(c+h)(c−h)(d+k)(d−k)(d+k)(d−k)
512
Spreading
Transmission
Despreading
code: (1,1,1,1)
[(a+f)+(a−f)+(a+f)+(a−f)] [(b+g)+(b−g)+(b+g)+(b−g)] [(c+h)+(c−h)+(c+h)+(c−h)] [(d+k)+(d−k)+(d +k)+(d−k)] = 4a4b4c4d = abcd
Spreading Factor: 4
code: (1,−1,1,−1)
[(a+f)−(a−f)+(a+f)−(a−f)] [(b+g)−(b−g)+(b+g)−(b−g)] [(c+h)−(c−h)+(c+h)−(c−h)] [(d+k)−(d−k)+(d+k)−(d−k)] = 4f4g4h4k = fghk
Spreading Factor: 4

FIG. 8

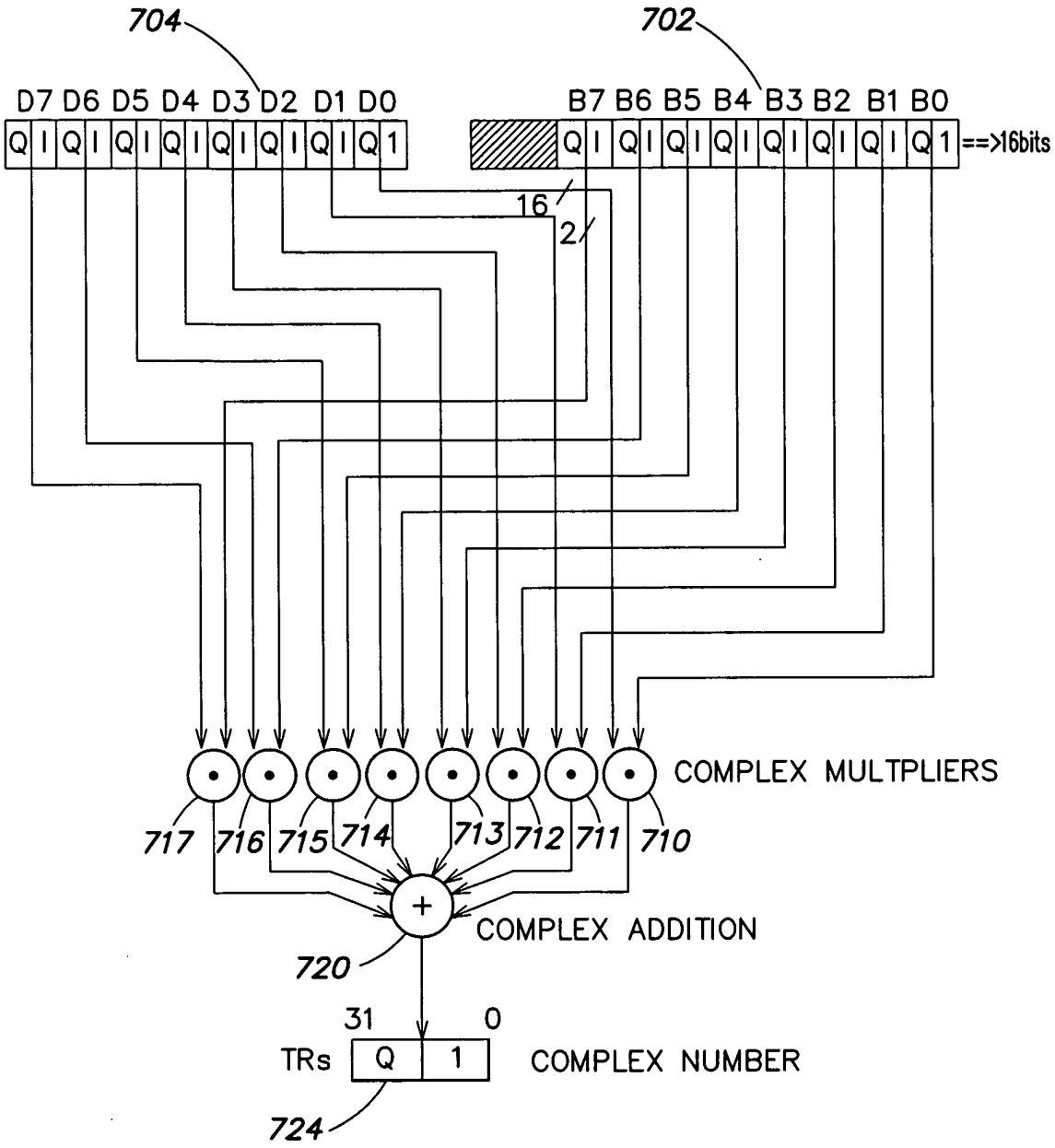
704
702
D7 D6 D5 D4 D3 D2 D1 D0
B7 B6 B5 B4 B3 B2 B1 B0
Q I Q I Q I Q I Q I Q I Q I Q 1
==>16bits
16
2
COMPLEX MULTPLIERS
717
716
715
714
713
712
711
710
+
COMPLEX ADDITION
720
31
0
TRs
Q
1
COMPLEX NUMBER
724

FIG. 9

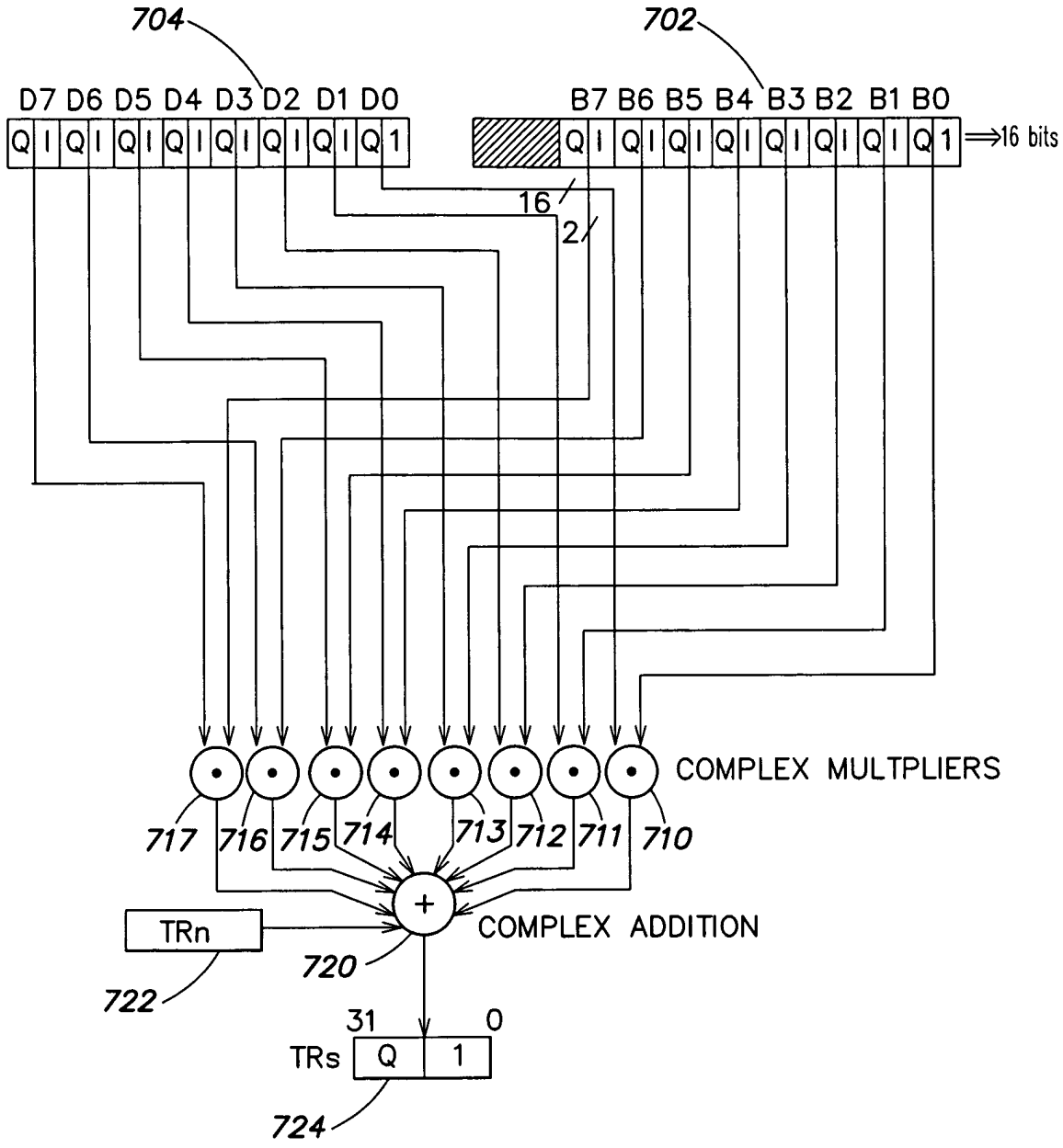
704
702
D7 D6 D5 D4 D3 D2 D1 D0
B7 B6 B5 B4 B3 B2 B1 B0
Q I Q I Q I Q I Q I Q I Q I Q 1
⟹16 bits
16
2
COMPLEX MULTPLIERS
717 716 715 714 713 712 711 710
+
COMPLEX ADDITION
TRn
720
722
31
0
TRs
Q
1
724

FIG. 10

```
    602
TR0 = DESPREAD (R3:0, THR1:0)          ; xR3:0 = SDAB Q[J0+=8];;
    604
xTR0 = DESPREAD (R7:4, THR1:0) + TR0; xR7:4 = SDAB Q[J0+=8];;
    606
xTR0 = DESPREAD (R3:0, THR1:0) + TR0; xR3:0 = SDAB Q[J0+=8];;
    608
xTR0 = DESPREAD (R7:4, THR1:0) + TR0; xR7:4 = SDAB Q[J0+=8];
    610
xTHR1:0 = R19:18 (I);;
```

FIG. 11

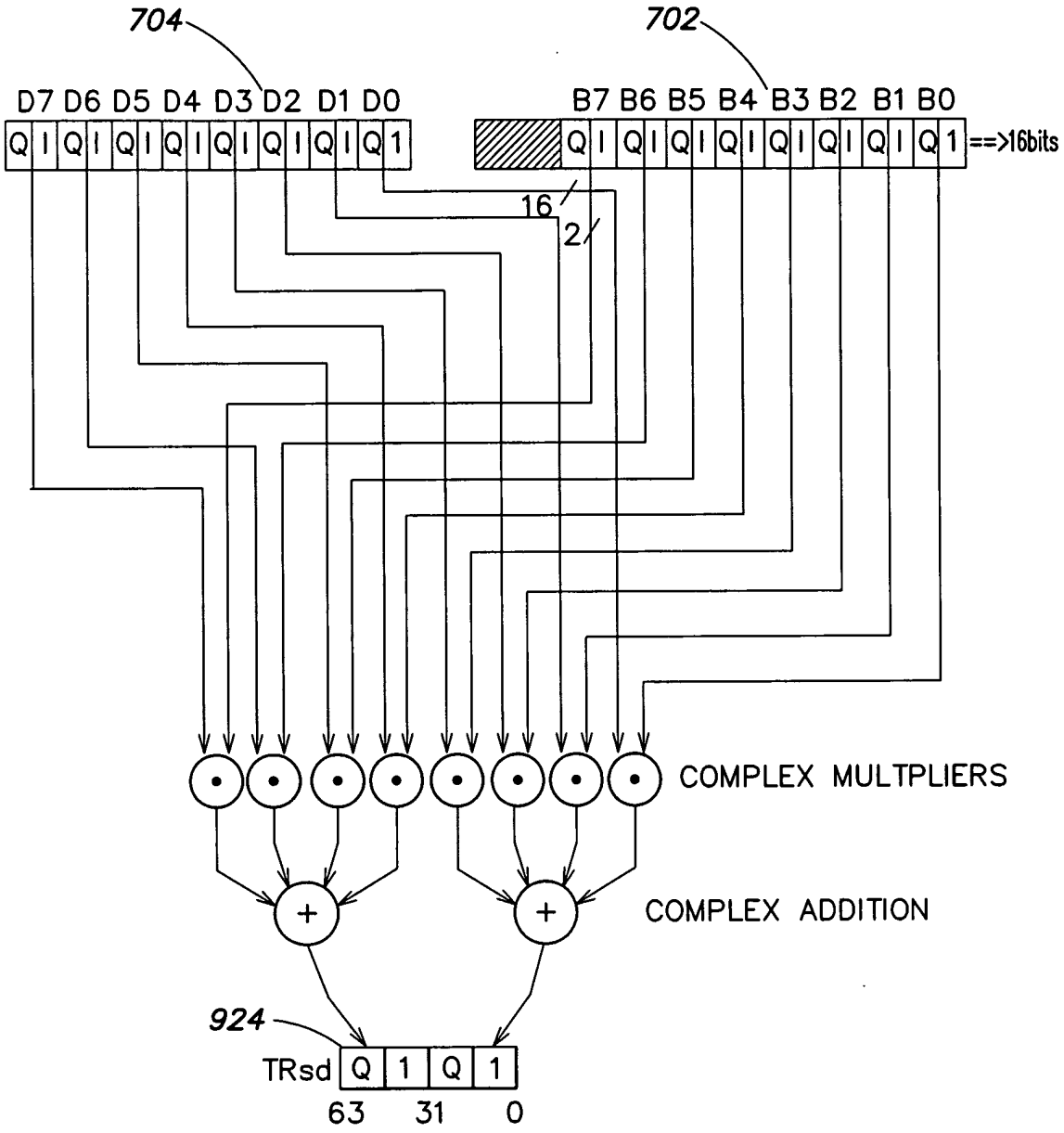
704
702
D7 D6 D5 D4 D3 D2 D1 D0
B7 B6 B5 B4 B3 B2 B1 B0
Q I Q I Q I Q I Q I Q I Q I Q 1
==>16bits
16
2
COMPLEX MULTPLIERS
COMPLEX ADDITION
924
TRsd
Q 1 Q 1
63 31 0

FIG. 12